11-08-00

JC962 U.S. PTO 11/07/00

09/707452 PTO 11/07/00

Please type a plus sign (+) inside this box → [+]

PTO/SB/05 (4/98)
Approved for use through 09/30/2000. OMB 0651-0032
Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 C.F.R. § 1.53(b))

Attorney Docket No.	TESSERA 3.0-051 FWC DIV
First Inventor or Application Identifier	Fjelstad
Title	SUBTRACTIVELY CREATED INTERCONNECTION METHOD AND APPARATUS
Express Mail Label No.	EL408439261US

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO: **Box Patent Application, Washington, DC 20231**

1. [X] * Fee Transmittal Form *(e.g., PTO/SB/17)* *(Submit an original and a duplicate for fee processing)*
2. [X] Specification [*Total Pages* 20]
   (preferred arrangement set forth below)
   - Descriptive title of the Invention
   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to Microfiche Appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings *(if filed)*
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
3. [X] Drawing(s) *(35 U.S.C. 113)* [*Total Sheets* 5]
4. Oath or Declaration [*Total Pages* 1]
   a. [ ] Newly executed (original or copy)
   b. [X] Copy from a prior application (37 C.F.R. § 1.63(d)) *(for continuation/divisional with Box 16 completed)*
      i. [ ] DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. §§ 1.63(d)(2) and 1.33(b).

** NOTE FOR ITEMS 1 & 13: IN ORDER TO BE ENTITLED TO PAY SMALL ENTITY FEES, A SMALL ENTITY STATEMENT IS REQUIRED (37 C.F.R. § 1.27), EXCEPT IF ONE FILED IN A PRIOR APPLICATION IS RELIED UPON (37 C.F.R. § 1.28).*

5. [ ] Microfiche Computer Program *(Appendix)*
6. Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
   a. [ ] Computer Readable Copy
   b. [ ] Paper Copy (identical to computer copy)
   c. [ ] Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

7. [ ] Assignment Papers (cover sheet & document(s))
8. [ ] 37 C.F.R.§3.73(b) Statement *(when there is an assignee)* [ ] Power of Attorney
9. [ ] English Translation Document *(if applicable)*
10. [X] Information Disclosure Statement (IDS)/PTO-1449 [ ] Copies of IDS Citations
11. [X] Preliminary Amendment
12. [X] Return Receipt Postcard (MPEP 503) *(Should be specifically itemized)*
13. [ ] * Small Entity Statement(s) *(PTO/SB/09-12)* [ ] Statement filed in prior application, Status still proper and desired
14. [ ] Certified Copy of Priority Document(s) *(if foreign priority is claimed)*
15. [ ] Other: .....

16. **If a CONTINUING APPLICATION**, *check appropriate box, and supply the requisite information below and in a preliminary amendment:*

[ ] Continuation [X] Divisional [ ] Continuation-in-part (CIP) of prior application No: 08/885,238

Prior application information: *Examiner* Chang, R. *Group / Art Unit:* 3729

For CONTINUATION or DIVISIONAL APPS only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 4b, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.

17. CORRESPONDENCE ADDRESS

[X] *Customer Number or Bar Code Label* 000530 *(Insert Customer No. or Attach bar code label here)* *or* [ ] *Correspondence address below*

Name					
Address					
City		*State*		*Zip Code*	
Country		*Telephone*		*Fax*	

Name (Print/Type)	WILLIAM SMITH	*Registration No. (Attorney/Agent)*	46,459
Signature		*Date*	11/7/2000

Burden Hour Statement: This form is estimated to take 0.2 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Box Patent Application, Washington, DC 20231.

PTO/SB/17 (08-00)
Approved for use through 10/31/2002 OMB 0651-0032
U S. Patent and Trademark Office, U S DEPARTMENT OF COMMERCE

FEE TRANSMITTAL for FY 2001

Patent fees are subject to annual revision.

TOTAL AMOUNT OF PAYMENT ($) 710.00

Complete if Known	
Application Number	
Filing Date	
First Named Inventor	Fjelstad
Examiner Name	Chang, R.
Group Art Unit	3729
Attorney Docket No.	TESSERA 3.0-051 FWC DIV

METHOD OF PAYMENT (check one)

1. [X] The Commissioner is hereby authorized to charge indicated fees and credit any overpayments to:

Deposit Account Number: 12-1095

Deposit Account Name: Lerner David et al.

[X] Charge Any Additional Fee Required Under 37 CFR 1 16 and 1 17

[ ] Applicant claims small entity status See 37 CFR 1 27

2. [ ] **Payment Enclosed:**

[ ] Check [ ] Credit card [ ] Money Order [ ] Other

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
101	710	201	355	Utility filing fee	710.
106	320	206	160	Design filing fee	
107	490	207	245	Plant filing fee	
108	710	208	355	Reissue filing fee	
114	150	214	75	Provisional filing fee	

SUBTOTAL (1) ($) 710.

2. EXTRA CLAIM FEES

		Extra Claims	Fee from below	Fee Paid
Total Claims	20	-20** = 0	X 0	= 0.
Independent Claims	1	- 3** = 0	X 0	= 0.
Multiple Dependent				=

**or number previously paid, if greater, For Reissues, see below

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
103	18	203	9	Claims in excess of 20
102	80	202	40	Independent claims in excess of 3
104	270	204	135	Multiple dependent claim, if not paid
109	80	209	40	** Reissue independent claims over original patent
110	18	210	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) 0.

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee or oath	
127	50	227	25	Surcharge - late provisional filing fee or cover sheet	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for *ex parte* reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for reply within first month	
116	390	216	195	Extension for reply within second month	
117	890	217	445	Extension for reply within third month	
118	1,390	218	695	Extension for reply within fourth month	
128	1,890	228	945	Extension for reply within fifth month	
119	310	219	155	Notice of Appeal	
120	310	220	155	Filing a brief in support of an appeal	
121	270	221	135	Request for oral hearing	
138	1,510	138	1,510	Petition to institute a public use proceeding	
140	110	240	55	Petition to revive - unavoidable	
141	1,240	241	620	Petition to revive - unintentional	
142	1,240	242	620	Utility issue fee (or reissue)	
143	440	243	220	Design issue fee	
144	600	244	300	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Petitions related to provisional applications	
126	240	126	240	Submission of Information Disclosure Stmt	
581	40	581	40	Recording each patent assignment per property (times number of properties)	
146	710	246	355	Filing a submission after final rejection (37 CFR § 1 129(a))	
149	710	249	355	For each additional invention to be examined (37 CFR § 1 129(b))	
179	710	279	355	Request for Continued Examination (RCE)	
169	900	169	900	Request for expedited examination of a design application	

Other fee (specify) _____

* Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($)

SUBMITTED BY				Complete (if applicable)	
Name (Print/Type)	WILLIAM SMITH	Registration No (Attorney/Agent)	46,459	Telephone	908-654-5000
Signature				Date	11/7/2000

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

Burden Hour Statement This form is estimated to take 0 2 hours to complete Time will vary depending upon the needs of the individual case Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, U S Patent and Trademark Office, Washington, DC 20231 DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS SEND TO Assistant Commissioner for Patents, Washington, DC 20231

PATENT
TESSERA 3.0-051 FWC DIV

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of Fjelstad	:	
	:	Group Art Unit: 3729
Divisional of Application No. 08/885,238	:	
	:	Examiner: Chang, R.
Filed: June 30, 1997	:	
For: SUBTRACTIVELY CREATED INTER-CONNECTION METHOD AND APPARATUS	:	Date: November 7, 2000

Assistant Commissioner for Patents
Washington, D.C. 20231

PRELIMINARY AMENDMENT

Sir:

It is respectfully requested that the above-identified application be amended as follows:

IN THE TITLE:

Change the title from "SUBTRACTIVELY CREATED INTERCONNECTION METHOD AND APPARATUS" to --CONNECTION COMPONENTS WITH POSTS--.

IN THE SPECIFICATION:

Page 1, insert before line 4:

--CROSS-REFERENCE TO RELATED APPLICATIONS

The present application is a divisional of co-pending Application Serial No. 08/885,238 filed on June 30, 1997, which is a continuation of Application Serial No. 08/366,236 filed on December 29, 1994.--

Page 5, line 8, after "1994," insert --which issued as U.S. Patent No. 5,445,390,--.

EXPRESS MAIL LABEL NUMBER: EL 408439261 US

Page 7, line 13, after "invention." insert:

--Figure 4A is an elevational view of a post and socket.

Figure 4B is a perspective view of a post and socket.--

Page 7, line 14, change "Figure 4" to read --Figure 5--.

Page 7, line 16, after "invention." insert:

--Figure 6A is an elevational view of a post.

Figure 6B is a top view of a brazing button and hole.--

IN THE CLAIMS:

Cancel claims 21 through 32.

Amend claim 1 as shown herein:

1. A method of fabricating interconnection members for a microelectronic device, the method comprising:

providing a support substrate having a first surface;

coupling a conductive sheet having a uniform thickness to the first surface of the support structure; and

selectively removing portions of the conductive sheet thereby producing a plurality of substantially rigid, [co-planar] elongated posts[.] protruding parallel to one another from the first surface of the support structure, each post having a base surface and a top surface, wherein each base surface is disposed on the substrate, the top surfaces being remote from the substrate and substantially coplanar with respect to one another.

Claim 3, line 12, replace "component" with --method--.

Amend claim 4 as shown herein:

4. The [component] method as claimed in claim 2, wherein [the] each post[s] [have] has a cooling tower shape[.], each post tapering inwardly from said base surface to a narrow region between the base surface and the top surface and flaring outwardly from said narrow region toward said top surface.

Claim 5, line 16, replace "component" with --method--.

Claim 8, line 23, delete [highly].

REMARKS

The present application is a divisional of co-pending Application No. 08/885,238 filed on June 30, 1997, which is a continuation of Application No. 08/366,236 filed on December 29, 1994, and contains no new matter over the prior applications. A copy of the executed Declaration filed in Application No. 08/366,236 is attached.

The present Preliminary Amendment cancels the claims previously elected in response to a restriction requirement in Application No. 08/885,238, and amends the remaining claims in accordance with comments received from the Examiner during prosecution of the parent application.

If there are any fees to be incurred in connection with this Preliminary Amendment, the Examiner is authorized to charge Deposit Account No. 12-1095.

Respectfully submitted,

LERNER, DAVID, LITTENBERG,
KRUMHOLZ & MENTLIK, LLP

WILLIAM SMITH
Reg. No. 46,459

600 South Avenue West
Westfield, NJ 07090-1497
Telephone: (908) 654-5000
Facsimile: (908) 654-7866

279680_1.DOC

SUBTRACTIVELY CREATED INTERCONNECTION METHOD AND APPARATUS

Field of the Invention

The present invention relates, generally, to interconnecting microelectronic devices and supporting substrates, and more particularly relates to an apparatus and a method of interconnecting microelectronic devices to supporting substrates using subtractively created members.

Background of the Invention

Complex microelectronic devices such as modern semiconductor chips require many hundreds of input and output connections to other electronic components. These device connections are generally either disposed in regular grid-like patterns, substantially covering the bottom surface of the device (commonly referred to as an "area array") or in elongated rows extending parallel to and adjacent each edge of the device's front surface. The various prior art processes for making the interconnections between the microelectronic device and the supporting substrate use prefabricated arrays or rows of leads/discrete wires, solder bumps or combinations of both, such as with wire bonding, tape automated bonding ("TAB") and flip/chip bonding.

In a wirebonding process, the microelectronic device may be physically mounted on a supporting substrate. A fine wire is fed through a bonding tool and the tool is brought into engagement with a contact pad on the device so as to bond the wire to the contact pad. The tool is then moved to a connection point of the circuit on the substrate, so that a small piece of wire is dispensed and formed into a lead, and connected to the substrate. This process is repeated for every contact on the chip. The wire bonding process is also commonly used to connect the die bond pads to lead frame fingers which are then connected to the supporting substrate.

In a tape automated bonding ("TAB") process, a dielectric supporting tape, such as a thin foil of polyimide is provided with a hole slightly larger than the microelectronic device. An array of metallic leads is provided on one surface of the dielectric film. These leads extend inwardly from around the hole towards the edges of the hole. Each lead has an innermost end projecting inwardly, beyond the edge of the hole. The innermost ends of the leads are arranged side by side at a spacing corresponding to the spacing of the contacts on the device. The dielectric film is juxtaposed with the device so that the hole is aligned with the device and so that the innermost ends of the leads will extend over the front or contact bearing surface on the device. The innermost ends of the leads are then bonded to the contacts of the device, typically using ultrasonic or thermocompression bonding, and the outer ends of the leads are connected to external circuitry.

In both wire bonding and conventional tape automated bonding, the pads on the substrate are arranged outside of the area covered by the chip, so that the wires or leads fan out from the chip to the surrounding pads. The area covered by the entire assembly is considerably larger than the area covered by the chip. This makes the entire assembly substantially larger than it otherwise would be. Because the speed with which a microelectronic assembly can operate is inversely related to its size, this presents a serious drawback. Moreover, the wire bonding and tape automated bonding approaches are generally most workable with chips having contacts disposed in rows extending along the edges of the chip. They generally do not allow use with chips having contacts disposed in an area array.

In the flip-chip mounting technique, the front or contact bearing surface of the microelectronic device faces towards the substrate. Each contact on the device is joined by a solder bond to the corresponding contact pad on the supporting substrate, as by positioning solder balls on the substrate or device, juxtaposing the device with the substrate in the front-face-down orientation and

momentarily reflowing the solder. The flip-chip technique yields a compact assembly, which occupies an area of the substrate no larger than the area of the chip itself. However, flip-chip assemblies suffer from significant problems when encountering thermal stress. The solder bonds between the device contacts and the supporting substrate are substantially rigid. Changes in the relative sizes of the device and the supporting substrate due to thermal expansion and contraction in service create substantial stresses in these rigid bonds, which in turn can lead to fatigue failure of the bonds. Moreover, it is difficult to test the chip before attaching it to the substrate, and hence difficult to maintain the required outgoing quality level in the finished assembly, particularly where the assembly includes numerous chips.

As the number of interconnections per microelectronic device increases, the issue of interconnection planarity continues to grow as well. If the interconnections are not planar with respect to each other, it is likely that many of the interconnections will not electrically contact their juxtaposed contact pads on a supporting substrate, such as a standard printed wiring board. None of the above described techniques provides a cost effective interconnection scheme which guarantees the planarity of the interconnections so that each is assured of making an electrical contact with the contact pads on the opposed supporting substrate.

Numerous attempts have been made to solve the foregoing interconnection problems. An interconnection solution put forth in U.S. Patent No. 4,642,889, entitled "Compliant Interconnection and Method Therefor" issued April 29, 1985 to Grabbe creates an interconnection scheme by embedding wires within each solder column/ball to reinforce the solder thereby allowing higher solder pedestals and more elasticity. Further interconnection solutions put forth include providing a combination of solder and high lead solder thereby allowing higher solder pedestals and more elasticity given the high lead content of the solder, as

found in U.S. Patent No. 5,316,788, entitled "Applying Solder to High Density Substrates" issued May 31,1994 to Dibble et al. and U.S. Patent No. 5,203,075 & 5,133,495, respectively issued on April 20, 1993 and July 28, 1992 to Angulas et al.

U.S. Patent No. 4,955,523, entitled "Interconnection of Electronic Components" issued on September 11, 1990 to Calomagno et al. puts forth a still further interconnection technique in which wires are wirebonded to the contact pads on a first surface, cut to a desired length and then attached to a second opposing surface by placing each of the wires in a "well" of conductive material, such as solder. While the wires then give a certain amount of compliancy to the structure, this technique encounters difficulties in controlling unwanted bending and electrical shorting of the wires prior to and during the coupling step in their respective solder wells. Similarly, U.S. Patent No. 5,067,007, entitled "Semiconductor Device having Leads for Mounting to a Surface of a Printed Circuit Board" issued November 19, 1991 to Kanji et al. discloses the use of stiff or deformable lead pins to increase the pin pitch and deal with problems stemming from thermal coefficient of expansion mismatches between the device and a printed circuit board. Besides the potential for bending and shorting of the pins as described above, the pins are individually attached to both the device and the printed circuit board by brazing or soldering making this a time consuming and less than optimum solution from a manufacturing point of view.

U.S. Patent No. 4,067,104, entitled "Method of Fabricating an Array of Flexible Metallic Interconnects for Coupling Microelectronic Components" issued on January 10, 1978 to Tracy uses an additive technique where the interconnections are created by providing a layer of photoresist, removing portions of the photoresist and depositing metal within the removed portions. By successively following this technique, a plurality of metalized columns are created

and coupled to opposing contact pads on a supporting substrate by a suitable method, such as flip chip bonding, cold welding, diffusion bonding or melting. The photoresist is then removed. However, interconnection planarity issues can become a problem when practicing the invention disclosed in the '104 patent. Further, the strength of each of the interconnection columns may be impeded due to the joining of the different layers of metal and to thermal cycling fatigue.

One commonly assigned invention, U.S. Patent Application No. 08/190,779, filed February 1, 1994, deals effectively, but specifically differently, with many of the problems encountered by the prior art. In one embodiment, the '779 application interconnects the device contact pads to the supporting substrate terminals by using leads which are coupled to the terminals in a conventional manner, such as by soldering, such that they extend substantially side by side. The unconnected ends are then coupled to the contact pads through the use of predetermined pressure and temperature conditions. A support layer is then disposed between the device and the supporting substrate and further surrounds and supports the leads. This structure effectively deals with thermal expansion mismatch and lead shorting problems.

Despite these and other efforts in the art, still further improvements in microelectronic interconnection technology would be desirable.

Summary of the Invention

The present invention provides a method and apparatus for providing interconnections between a microelectronic device and a supporting substrate which substantially obviates many of the problems encountered by the prior art.

One embodiment of the present invention provides a method of fabricating an interconnection component for a microelectronic device comprises providing a support structure, typically comprised of a flexible but substantially inextensible substrate, having a first and a second surface, where a conductive

sheet is coupled to the first surface of the support structure. The conductive sheet is then selectively removed, typically using an etching process, thereby producing a highly planar, cost effective plurality of substantially rigid posts each of which eventually become the interconnections between the microelectronic device and a supporting substrate. The etching process generally first includes applying a photoresist layer to the conductive sheet and exposing portions of the photoresist layer to form etch resistant portions and remainder portions. The remainder portions may then be removed and the conductive sheet may be etched around the etch resistant portions.

A compliant layer may then be provided on the second surface of the support structure and a microelectronic device having a plurality of bond pads may be engaged with the exposed surface of the compliant layer. The compliant layer is used to substantially accommodate thermal coefficient of expansion mismatches between the device and a supporting substrate when the device is in use. Each bond pad is then electrically coupled to at least one conductive post. The bond pads and posts may be coupled in a number of different ways, including plating a plurality of etch resistant conductive leads on either the first surface of the support structure or the conductive sheet such that the leads are sandwiched between the supporting substrate and the conductive sheet. After the posts are created, the bond pads may be electrically connected to respective leads. Alternately, the conductive leads could be formed on the second surface of the support structure and coupled to each post through a conductive via. A highly conductive layer, such as gold, may optionally be plated on the surface of the posts to ensure a good electrical connection when the posts are coupled to contact pads on a supporting substrate.

The foregoing and other objects and advantages of the present invention will be better understood from the following Detailed Description of a Preferred Embodiment, taken together with the attached Figures.

Brief Description of the Drawings

Figures 1A and 1B are perspective views illustrating the process of subtractively creating the interconnections according to one embodiment of the present invention.

Figures 2A and 2B are perspective views each showing the embodiment in Figure 1B coupled to a compliant layer and a microelectronic device according to one embodiment of the present invention.

Figures 3A-C are perspective views each showing one possible shape of the subtractively created interconnections according to the present invention.

Figure 4 is a perspective view of a subtractively created interconnection having an etch resistant, conductive cap thereon according to the present invention.

Detailed Description of a Preferred Embodiment

Referring to Figures 1A and 1B, a top surface of a support structure 100 is coupled to a conductive sheet 110. In the preferred embodiment of the invention, the support structure is a flexible, but substantially inextensible, film preferably formed from a polymeric material , such as Kapton™, of an approximate thickness between 25 microns and 75 microns and is laminated to the second surface of the conductive sheet. However, the support structure could be comprised of many other suitable materials and may further be semi-flexible or substantially rigid. The conductive sheet 110 is preferably comprised of a conductive metal, such as copper, copper alloys or phosphor bronze, among other materials. Portions of the conductive sheet are selectively removed by any suitable

means to create a plurality of subtractively created, substantially rigid posts 130, as shown in Figure 1B.

In the preferred embodiment, portions of the conductive sheet are removed by first providing a photoresist mask on the surface of the conductive sheet and etching away the conductive sheet 110 around the mask portions. This is preferably accomplished by coupling a photoresist layer 120 to the top surface of the conductive sheet 110. Selected portions of the photoresist layer 120 are then exposed and developed using standard industry techniques, resulting in a plurality of etch resistant photoresistive portions 125 atop the conductive sheet 100. A one sided etching process is then employed to remove portions of the conductive sheet 110 around the plurality of etch resistant photoresistive portions 125 while substantially leaving the portions beneath the plurality of etch resistant photoresistive portions 125, as shown in Figure 1B. The etch profile of features created from a conductive sheet, such as a metal foil, can be influenced by the process used to produce them. The two most common methods of etching are batch immersion in an etchant solution and liquid etchant spraying or impingement. In batch etching, the features can be more uniformly created. Etching proceeds isotropically removing metal at a basically uniform rate both vertically and laterally. This results in creating posts having substantially uniformly sloping vertical sides of approximately a 45° angle relative to the surface of the support structure. Etching normally proceeds rather slowly in batch processing providing sufficient time to replenish the active etchant solution to foil under the resist. In contrast, a spray etching technique typically impinges the part at more of a 90° angle, facilitating the etching of surfaces exposed to the impingement. While the etching process still progresses in a more or less isotropic fashion, the etch resistant photoresist portions 125 act as a shield causing the etching process to produce an etch profile which forms "cooling tower" shaped posts 130 having a broad base which thins as it

reaches the vertical center of the post 130 and flares back out slightly as it reaches its apex. These features are caused by the "splash back" of the etchant solution against the walls of the emerging post and can be more or less exaggerated by altering the pressure, concentration and or formula of the etchant within the bounds of the photoresist's resistance to the etchant.

The height of each post will vary directly with the thickness of the conductive sheet 110, but typically will be in the range of 125 to 500 microns. Because of their shape and rigidity, the conductive posts 130 will resist deformation. A fine post connect pitch can therefore be created without substantial fear that the posts 130 will be bent into electrical contact with each other. The possible pitch of the bumps is also a function of the thickness of the sheet of conductive material. The thinner the conductive sheet, the finer the possible pitch of the bumps. Also, this process of creating the posts is cost and time effective when compared with methods which create each bump by plating or soldering. Further, the posts created with this subtractive process are extremely uniform and planar when compared to solder or plated bumps because they are created from a single planar, conductive sheet. This ensures that each of the bumps will make contact with respective contact pads on a supporting substrate, such as a printed wiring board, without the exertion of undue pressure on the top surface of the microelectronic device.

The exterior surfaces of the posts may be optionally plated with a highly conductive layer, such as gold, gold/nickel, gold/osmium or gold/palladium, or alternately plated with a wear resistant, conductive coating such as osmium to ensure that a good connection is made when the posts are either soldered or socketed to a supporting substrate, as described more fully below.

Referring now to Figure 2A, a compliant layer 140 is coupled to the back surface of the support structure 100. The compliant layer 140 is typically

made of an elastomer material, such as the Dow Corning silicon elastomer 577 known as Silgard®. The compliant layer 140 is coupled to the back surface of the support structure 100 by conventional stencil printing techniques. The silicon elastomer used in the preferred embodiment is filled with about 5-10% of fumed silica in order to obtain a stiff consistency that allows the layer 140 to retain its shape after the stencil is removed. The silicon is then cured at a suitable temperature. Typically, the thickness of the complaint layer is 150 microns, plus or minus 12.5 microns. The compliant layer 140 may alternately be replaced with a plurality of compliant pads 145 each positioned beneath a respective post, as shown in Figure 2B. The pads 145 are also typically stenciled on the back surface of the support structure 100 and the original stiff formulation of the elastomer allows each individual pad 145 to retain its shape after the stencil has been removed. The exposed surface of the compliant layer is next engaged with a surface of a microelectronic device 150 having a plurality of bond pads 160 thereon.

Referring now to Figure 2B, before the bond pads 160 can be connected to the conductive posts 130, a method of electrically connecting the posts 130 to the bond pads 160 must be supplied. One method includes providing etch-resistant conductive leads 170, such as copper leads which have been lithographically formed on the top surface of the support structure 100 plated with gold prior to coupling the structure 100 to the conductive sheet 110. After the conductive sheet 110 has been reduced to the conductive posts 130, shown in Figure 2A, the etch resistant conductive leads may be connected to the bond pads 160 by any suitable manner, such as wire bonding or by allowing the leads to extend beyond the edge of the support structure such that they may be bent towards and thermosonically or ultrasonically bonded to a respective bond pad, as shown in Figure 2A. An alternate method of creating a similar embodiment is to first plate a plurality of either one layer or a multi-layer etch resistant conductive leads,

such as gold or gold/copper leads, to the bottom surface of the conductive sheet 110 prior to coupling the conductive sheet 110 and the support structure 100. Portions of the conductive sheet are then removed to create the conductive posts 130 allowing the bond pads 160 to be electrically connected to the posts 130 by the conductive leads. A further alternate solution involves forming the leads on the second side of the support structure 100 and connecting the posts through conductive vias extending from the first to the second surface of the support structure 100.

A further embodiment of the present invention, includes directly attaching the support structure 100 to the microelectronic device such that each post is in electrical contact with a juxtaposed bond pad on the microelectronic device. This is typically accomplished using a conductive via positioned beneath each of the posts and extending from a first to a second surface of the support structure. The via may be created by punching or laser ablating holes in the support structure and plating a conductive metal, such as copper into each of the holes. A joining layer, such as a gold/tin or silver/tin alloy, is next typically coupled to the copper. The joining layer will weld to its respective bond pad under the correct temperature, pressure or vibration stresses.

As stated above, the shape of the posts 130 can depend on the process used to remove the surrounding conductive material. However, the shape of the etch resistant photoresist portions 125 in Figure 1A may also produce different shaped posts from the conductive sheet material. For example, Figure 3A shows a substantially in the form of a surface of revolution which is the result of using circular resist portions 180 on the conductive sheet 110. Square resist portions 190 will produce a post having four slightly concave, rounded sides meeting at slightly rounded edges, as shown in Figure 2B. Triangular resist portions 200 will produce a post having three slightly concave, rounded sides meeting at

slightly rounded edges, as shown in Figure 2C. Each of these photoresist portions produce the "cooling tower" shape shown if a spray etching process is used. If a batch immersion process is used, the resulting posts will have more linearly sloping vertical walls and slightly sharper corners.

The peaks of the posts 130 may then be coupled to the contact pads on the supporting substrate by any suitable means, such as directly soldering the posts to the contact pads or inserting them into sockets attached to the substrate. The "cooling tower" shape created by spray etching makes for a more reliable leaf-spring socket connection because its peak has a larger diameter than its middle section, as shown in Figure 4A. The peak of the post will thus provide resistance to being pulled out of the socket in response to forces acting in the lengthwise plane of the posts. The vertical corners on the posts shown in Figures 3B and 3C partially inserted into round socket holes or vias also makes for a more reliable, force fit, separable, electrical connection with each socket hole contact, as shown in Figure 4B.

Figure 5 shows a further embodiment in which the photoresist layer 120, in Figure 1, is replaced with a plurality of metallic portions 210 of a geometry similar to the photoresist portions (180/190/200) in Figures 3A-C. Typically, the metallic portions 210 are comprised of an etch resistant metal, such as nickel. The conductive layer may then be etched around the metallic portions 210 leaving the post capped with a conductive top. This conductive top may then be plated with a highly conductive layer, such as gold or a gold alloy. This conductive top further increases the reliability of an electrical connection when the posts are inserted into the type of socket shown in Figure 4A. In an alternate embodiment, solder can also be used as an etch resist. After the posts are created, the solder can then be reflowed to create a solder coated post. If the solder is reflowed after the post has

been inserted into a test socket, it will create a more permanent electrical connection with the socket.

Figures 6A-B show a still further embodiment having a brazing button 220 extending through brazing hole in a removable support structure 230. The brazing button is used to attach the post directly to a bond pad on a microelectronic device and is typically comprised of a metallic alloy which will attach easily and provide a good electrical connection with its respective bond pad, such alloys include gold-tin, bismuth-tin, gold-silicon, or tin-silver. Figure 6B shows one embodiment of a brazing hole 240 which allows for expansion of the brazing button when it is heated to attach to the chip bond pad. The removable support structure 230 is comprised of a material which may be removed by any suitable means after the posts have been attached to the bond pads, such as using a paper or water soluble polymeric support structure which may be sprayed with water and peeled off.

One skilled in the art will appreciate that the subtractively created posts described herein could be used for many other purposes besides connecting microelectronic devices to supporting substrates without departing from the spirit of the present invention. Further, if the top surfaces of the posts are sufficiently wide, a cupped portion could be provided thereon to receive bumps or solder balls on the surface of a supporting substrate.

Having fully described several embodiments of the present invention, it will be apparent to those of ordinary skill in the art that numerous alternatives and equivalents exist which do not depart from the invention set forth above. It is therefore to be understood that the present invention is not to be limited by the foregoing description, but only by the appended claims.

What is claimed is:

1. A method of fabricating interconnection members for a microelectronic device, the method comprising:

providing a support substrate having a first surface;

coupling a conductive sheet having a uniform thickness to the first surface of the support structure; and

selectively removing portions of the conductive sheet thereby producing a plurality of substantially rigid, coplanar posts.

2. The method as claimed in claim 1, wherein the support substrate is a flexible dielectric substrate.

3. The component as claimed in claim 2, wherein each post has at least one edge extending along the post in its direction of elongation.

4. The component as claimed in claim 2, wherein the posts have a cooling tower shape.

5. The component as claimed in claim 4, wherein each post has at least one edge extending along the post in its direction of elongation.

6. The method as claimed in claim 2, wherein the conductive sheet is selected from the group consisting of copper, brass, and bronze.

7. The method as claimed in claim 6, wherein the conductive sheet has a thickness between 125 and 500 microns.

8. The method as claimed in claim 7, further comprising plating a highly conductive layer to the exposed surface of each of the posts.

9. The method as claimed in claim 1, wherein the step of selectively removing comprises:

providing etch-resistant portions to a second surface of the conductive sheet remote from the dielectric substrate;and

etching the conductive sheet, the etch-resistant portions being substantially unaffected by the etching process.

10. The method as claimed in claim 9, wherein the providing etch resistant portions step includes:

applying a photo resist layer to the conductive sheet;

selectively developing the photoresist layer to form etch resistant portions and remaining portions; and

removing remaining portions of the photoresist layer.

11. The method as claimed in claim 1, further comprising:

providing a microelectronic device having a plurality of bond pads on a first surface above a second surface of the dielectric sheet remote from the posts; and

electrically connecting each bond pad to one post.

12. The method as claimed in claim 11, further comprising disposing a compliant layer between the second surface of the dielectric sheet and the first surface of the microelectronic device.

13. The method as claimed in claim 12, further comprising soldering an apex portion of each post to a contact on a printed circuit board.

14. The method as claimed in claim 12, further comprising disposing each post within and in electrical contact with a respective socket on a printed circuit board.

15. The method as claimed in claim 11, wherein the step of electrically connecting including:

providing a plurality of conductive vias extending from the first to the second surface of the dielectric substrate, each via positioned beneath and in electrical contact with one post;

connecting each bond pad to a respective post through a respective conductive via.

16. The method as claimed in claim 15, wherein the connecting step includes providing brazing buttons each extending from one via and coupling each brazing button to a bond pad on a chip.

17. The method as claimed in claim 16, further comprising the step of removing the support substrate after the brazing buttons have been attached to the bonding pads.

18. The method as claimed in claim 9, wherein the etch resistant portions include metallic portions.

19. The method as claimed in claim 18, wherein the metallic portions are comprised of nickel.

20. The method as claimed in claim 19, further comprising the step of coupling a highly conductive layer to each of the metallic portions.

21. A connection component, comprising:

a support substrate having a first surface;

a plurality of substantially rigid, elongated posts protruding parallel to one another from the first surface of the support substrate, each post having a base surface and a top surface, wherein each base surface is disposed adjacent the substrate, the top surfaces being remote from the substrate and substantially coplanar with respect to one another, the base surface of each post further having a greater width than the top surface thereof.

22. The component as claimed in claim 21, wherein the support substrate includes a flexible dielectric substrate.

23. The component as claimed in claim 21, wherein the posts have a cooling tower shape.

24. The component as claimed in claim 21, wherein each post has at least one edge extending along the post in its direction of elongation.

25. The apparatus as claimed in claim 21, wherein the posts have a collective height between 125 and 150 microns.

26. The component as claimed in claim 21, wherein a highly conductive layer is plated to the exposed surface of each of the posts.

27. The component as claimed in claim 21, further comprising:

a microelectronic device having a plurality of bond pads on a first surface, wherein the device is disposed above a second surface of the support substrate remote from the posts; and

means for electrically coupling each bond pad to at least one post.

28 The component as claimed in claim 27, further comrising a compliant layer disposed between the second surface of the dielectric sheet and the first surface of the microelectronic device.

29. The component as claimed in claim 27, further comprising:

the support substrate further having a plurality of conductive vias extending from the first to the second surface of the support structure beneath and in electrical connection with each of the posts, wherein the for electrically coupling includes connecting each bond pad to one post through one respective via.

30. The component as claimed in claim 21, further comprising a metallic member overlying the top surface of each post,

31. The component as claimed in claim 30, wherein each metallic member has a greater width than the width of the top surface of its respective post.

32. The component as claimed in claim 31, wherein a highly conductive layer is coupled to each of the metallic members.

33. A method of electrically connecting a microelectronic component having a first surface bearing a plurality of contacts comprising the steps of:

forming a subassembly by juxtaposing a connection component having a support structure and a plurality of elongated posts extending substantially parallel to one another from a first surface of the support structure with the microelectronic component so that the support structure overlies the first surface of the component with the posts extending away from the component, and electrically connecting the posts to the contacts of the microelectronic component; and

engaging the subassembly with a connector including a plurality of electrically conductive sockets each having an internal opening so that each post extends into the internal opening of one socket and each post is mechanically engaged with such socket.

34. The method as claimed in claim 33, wherein each post has one or more edges extending along the post in its direction of elongation and wherein each post engages the mating socket at such edges.

35. The method as claimed in claim 34, wherein each socket is a via having a conductive lining substantially in the form of a surface of revolution about an axis, each post extending substantially parallel to the axis of the engaged via lining, each post distorting the engaged via lining.

36. The method as claimed in claim 33, wherein each post has a surface flaring outwardly, transversely to the direction of elongation of the post

adjacent the support structure, the outwardly-tapering surfaces of the post engaging the sockets.

37. The method as claimed in claim 33, wherein the support structure includes a flexible sheet, the posts being attached to the flexible sheet, the step of forming a subassembly being conducted so that the posts can be moved relative to one another by flexure of the sheet.

38. The method as claimed in claim 37, wherein the step of forming a subassembly includes the step of providing a compliant material between the flexible sheet and the front surface of the microelectronic component.

ABSTRACT

A subtractively created interconnection scheme and apparatus, typically used with microelectronic devices, wherein a flexible support structure is attached to a conductive sheet. The conductive sheet is then selectively removed, preferably using an etching process, thereby producing a plurality of posts with tips which are substantially coplanar with respect to one another. Each post becoming an individual interconnection between the microelectronic device and a supporting substrate.

FIG. 1A

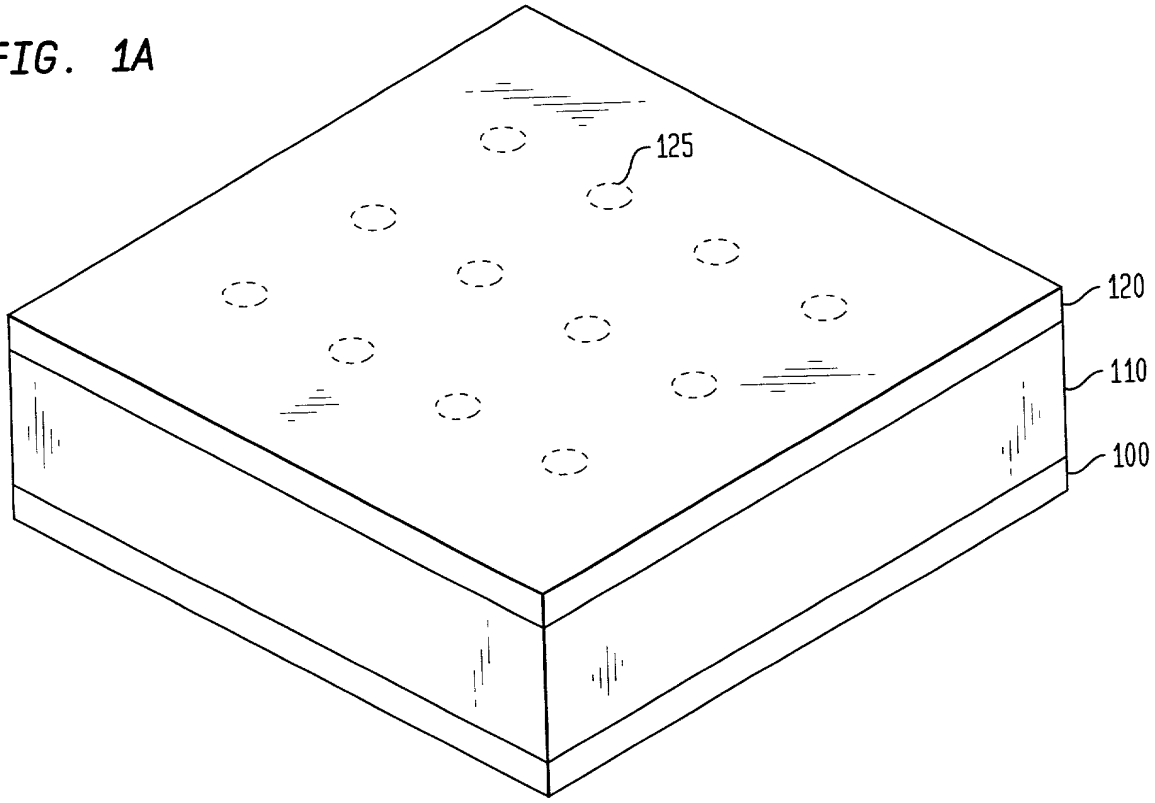


FIG. 1B

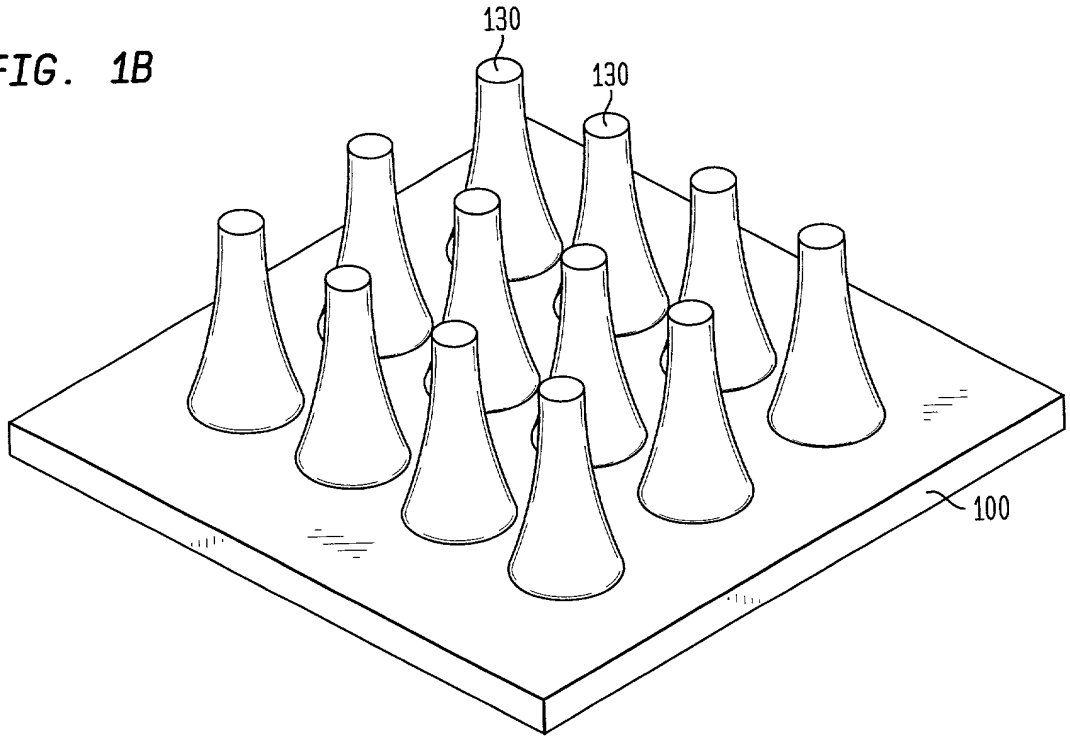


FIG. 2A

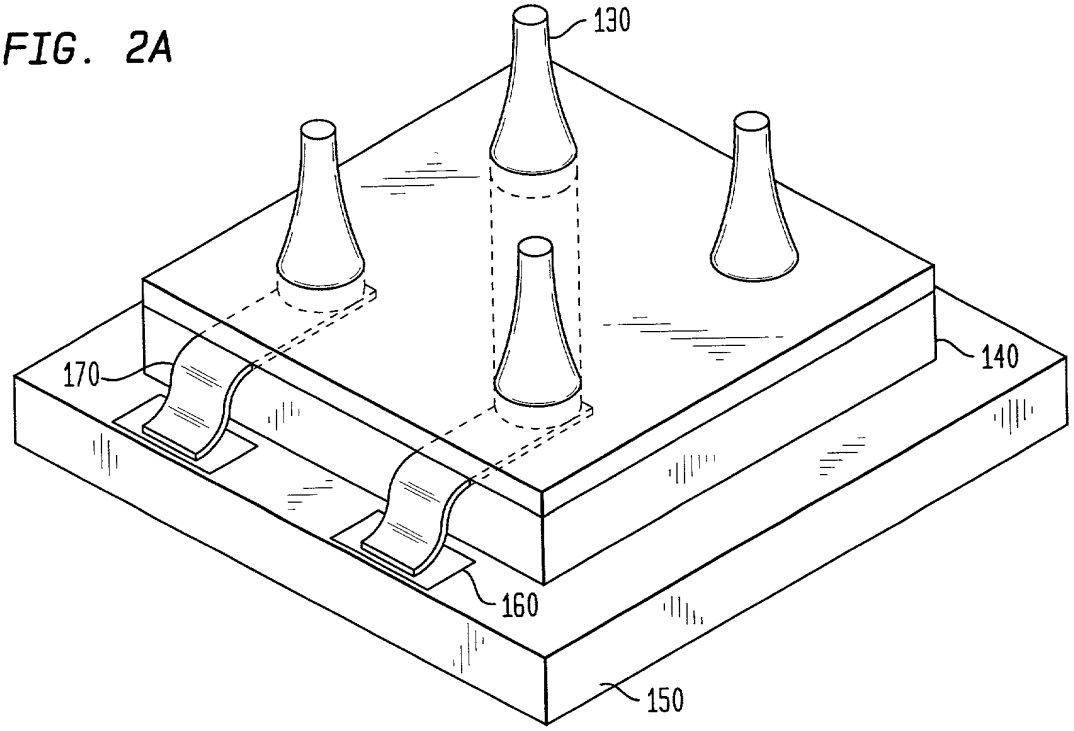


FIG. 2B

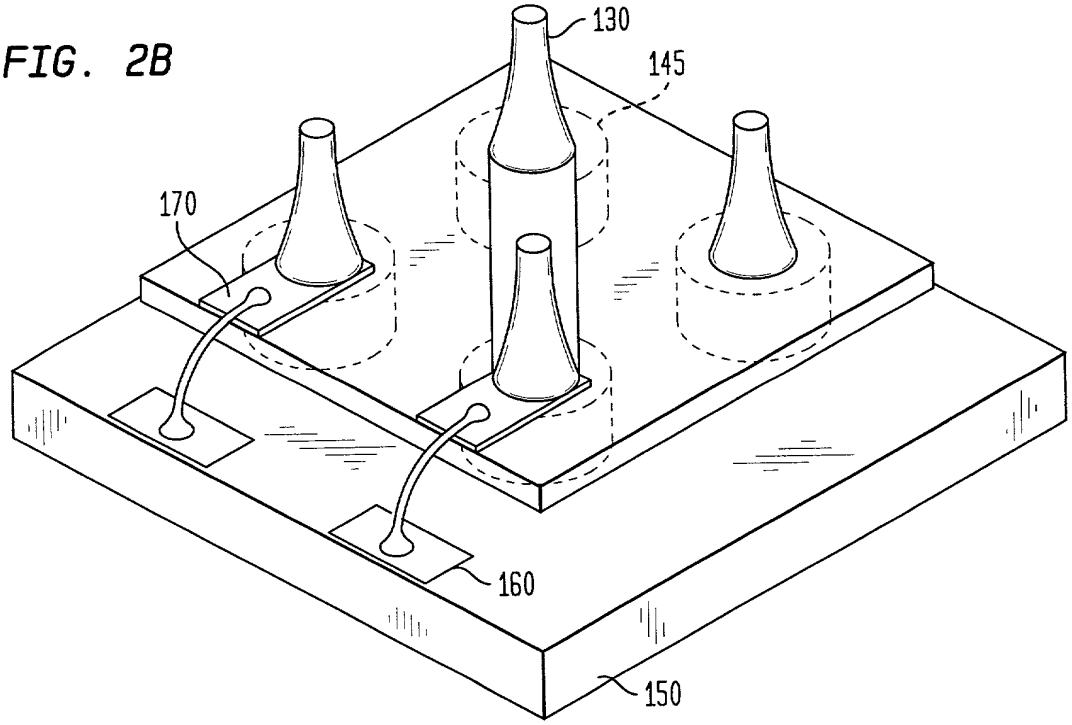


FIG. 3A

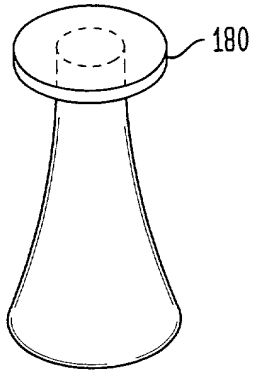


FIG. 3B

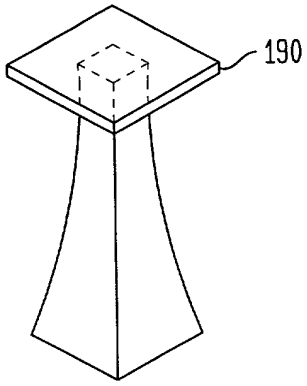


FIG. 3C

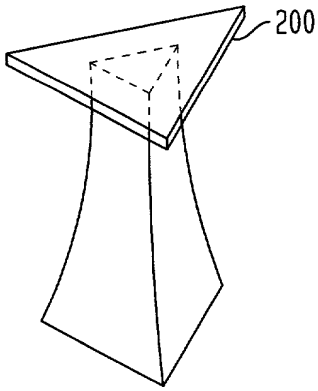


FIG. 4A

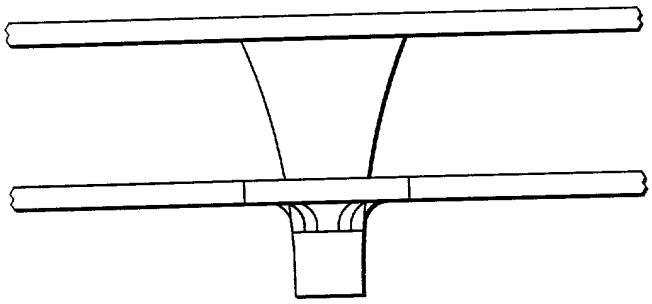


FIG. 4B

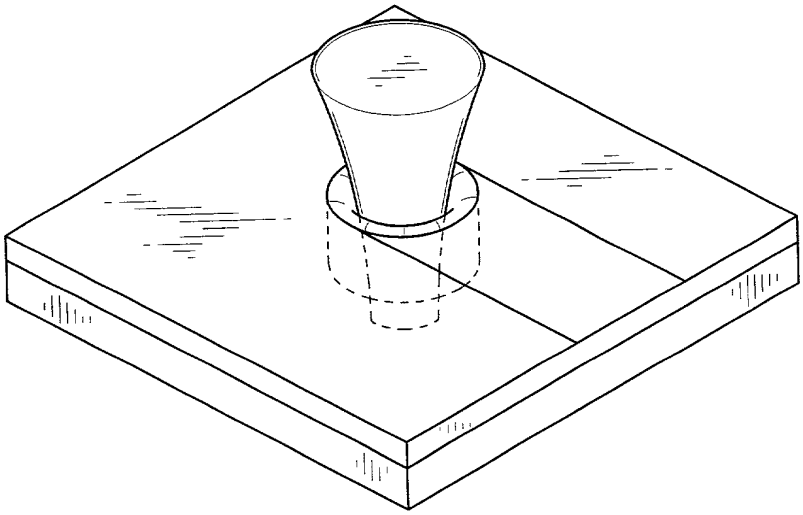


FIG. 5

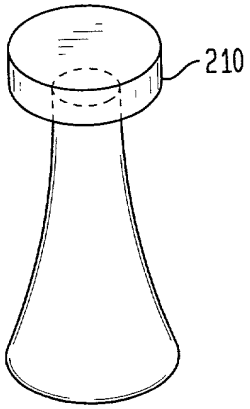


FIG. 6A

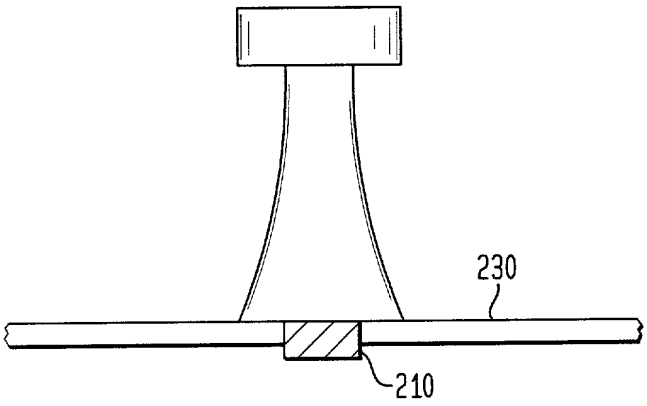
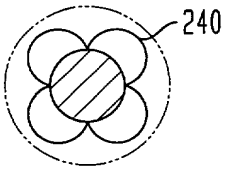


FIG. 6B



DECLARATION AND POWER OF ATTORNEY
(Patent, Design, or C-I-P Application)

ATTORNEY'S DOCKET NO.
Tessera 3.0-051

As a below-named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name;

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

SUBTRACTIVELY CREATED INTERCONNECTION METHOD AND APPARATUS

the specification of which

☒ is attached hereto

☐ was filed on _____ as Application Serial No. _____ and was amended on _____ (if applicable)

☐ was described and claimed in International Application No. _____ filed _____ and as amended on _____ (if any)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, § 1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, § 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

PRIOR FOREIGN APPLICATION(S)			
COUNTRY	APPLICATION NUMBER	DATE OF FILING (day, month, year)	PRIORITY CLAIMED UNDER 35 U.S.C. 119
			YES ☐ NO ☐
			YES ☐ NO ☐
			YES ☐ NO ☐

LISTING OF FOREIGN APPLICATIONS CONTINUED ON PAGE 2 HEREOF: ☐ YES ☒ NO

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)
(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)

LISTING OF US APPLICATIONS CONTINUED ON PAGE 2 HEREOF: ☐ YES ☒ NO

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith.

Lawrence I. Lerner, Reg. No. 19,516; Sidney David, Reg. No. 22,768; Joseph S. Littenberg, Reg. No. 20,832; Arnold H. Krumholz, Reg. No. 25,428; William L. Mentlik, Reg. No. 27,108; John R. Nelson, Reg. No. 26,573; Roy H. Wepner, Reg. No. 28,350; Stephen B. Goldman, Reg. No. 28,512; Paul H. Kochanski, Reg. No. 29,660; Marcus J. Millet, Reg. No. 28,241; Bruce H. Sales, Reg. No. 32,793; Daniel H. Bobis, Reg. No. 16,694; Peter J. Butch III, Reg. No. 32,203; Keith E. Gilman, Reg. No. 32,137; Robert B. Cohen, Reg. No. 32,768; Arnold B. Dompieri, Reg. No. 29,736; Michael H. Teschner, Reg. No. 32,862; Jeffrey S. Dickey, Reg. No. 35,858; Gregory S. Gewirtz, Reg. No. 36,522; Jonathan A. David, Reg. No. 36,494, Shawn P. Foley, Reg. No. 33,071; Lawrence G. Fridman, Reg. No. 31,615; Eileen Napolitano, Reg. No. 37,897; Christopher M. Pickett, Reg. No. 37,531.

SEND CORRESPONDENCE TO:	DIRECT TELEPHONE CALLS TO: (name and telephone number)
LERNER, DAVID, LITTENBERG, KRUMHOLZ & MENTLIK 600 South Avenue West Westfield, New Jersey 07090	(908) 654-5000

		LAST NAME	FIRST NAME	MIDDLE NAME
201	FULL NAME OF INVENTOR	FJELSTAD	JOSEPH	C.
	RESIDENCE & CITIZENSHIP	CITY: SUNNYVALE	STATE OR FOREIGN COUNTRY: CA	COUNTRY OF CITIZENSHIP: USA
	POST OFFICE ADDRESS	POST OFFICE ADDRESS: 1168 Vasquez, #1	CITY: SUNNYVALE	STATE OR COUNTRY: CA — ZIP CODE: 94086
202	FULL NAME OF INVENTOR	LAST NAME	FIRST NAME	MIDDLE NAME
	RESIDENCE & CITIZENSHIP	CITY	STATE OR FOREIGN COUNTRY	COUNTRY OF CITIZENSHIP
	POST OFFICE ADDRESS	POST OFFICE ADDRESS	CITY	STATE OR COUNTRY — ZIP CODE
203	FULL NAME OF INVENTOR	LAST NAME	FIRST NAME	MIDDLE NAME
	RESIDENCE & CITIZENSHIP	CITY	STATE OR FOREIGN COUNTRY	COUNTRY OF CITIZENSHIP
	POST OFFICE ADDRESS	POST OFFICE ADDRESS	CITY	STATE OR COUNTRY — ZIP CODE

LISTING OF INVENTORS CONTINUED ON PAGE 2 HEREOF: ☐ YES ☒ NO

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

SIGNATURE OF INVENTOR 201*	SIGNATURE OF INVENTOR 202*	SIGNATURE OF INVENTOR 203*
DATE: 12/22/94	DATE	DATE

SEE PAGE 2 ATTACHED, SIGNED AND MADE A PART HEREOF: ☐ YES ☒ NO

*Where use of Page 2 of this Declaration is necessary, only Page 2 is signed.